EPSON TOYOCOM

Application Manual

Real Time Clock Module

RTC-9701JE

Model	Product Number
RTC-9701JE	Q41970171000100

EPSON TOYOCOM CORPORATION

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Contents

Serial RTC Module with EEPROM

RTC - 9701JE

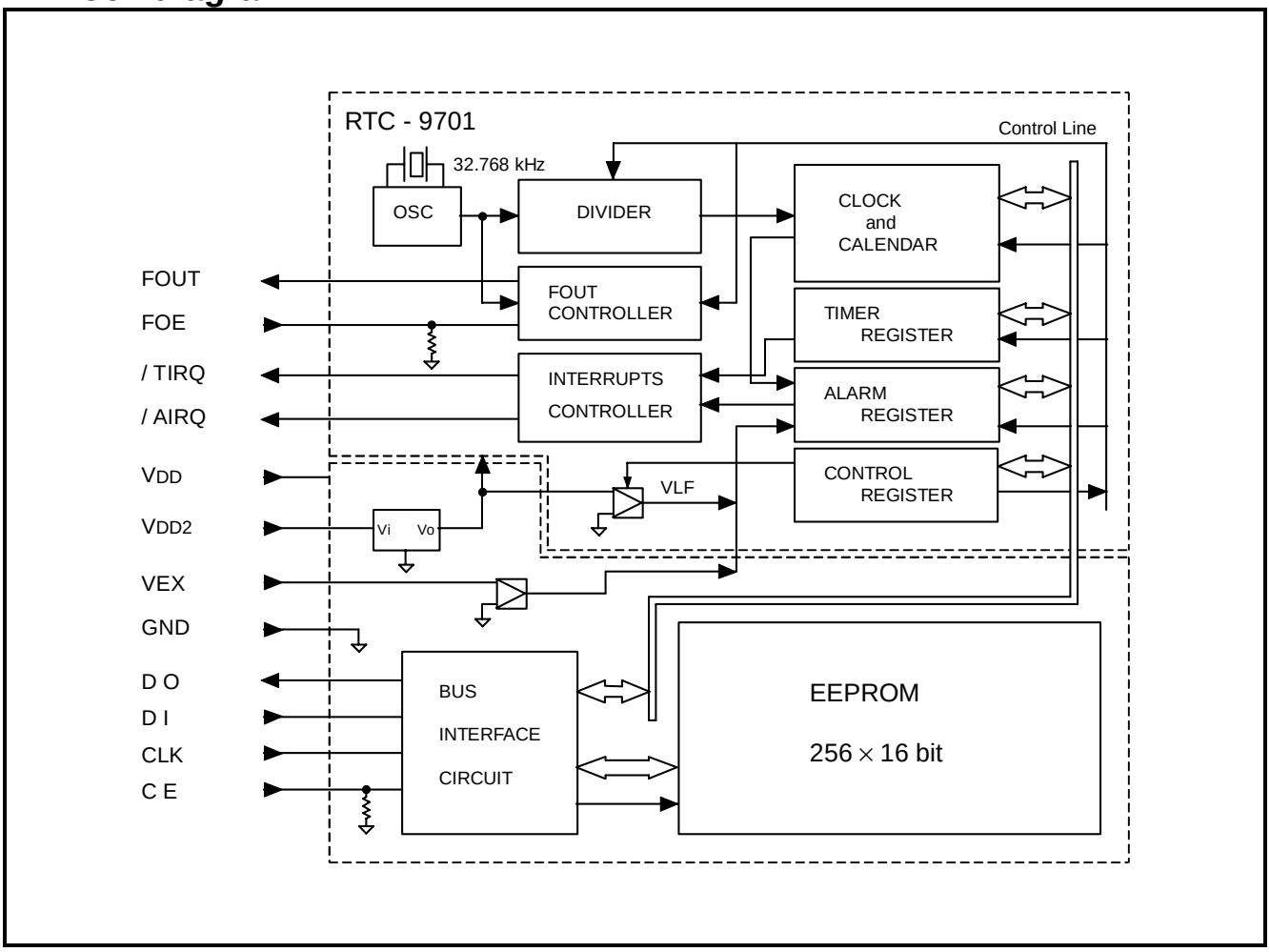
- Built-in 32.768 kHz crystal oscillator with frequency adjusted
- Alarm interrupt function for day of the week, day, hour, and minute
- Interval timer interrupt function
- Voltage decrease alarm function
- Time update alarm function
- Automatic adjustment for leap year
- Voltage detection function
- Nonvolatile 4 kbit (256×16 bit) memory
- Main power supply (V_{DD}) 2.7 V ~ 3.6 V
- Backup power supply (V_{DD2}) 1.8 V ~ 5.5 V
- Low current consumption at 0.8 µA / 3 V (Typ.)
- Available as small package (JE : VSOJ-20 pin)

1. Overview

This module is a high precision RTC module with serial interface in 4 lines form (or 3 lines form). It has a built-in 32.768 kHz crystal oscillator.

The system IC in the package has a variety of built-in functions such as high precision clock circuitry, crystal oscillator, 32.768 kHz output, nonvolatile memory, voltage detection circuitry, alarm and timer.

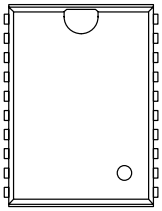
2. Block diagram



3. Terminal description

3.1. Terminal connections

RTC - 9701 JE

1.	V_{DD2}			20.	N.C.
2.	VEX	# 1		#20	19.	N.C.
3.	FOE				18.	N.C.
4.	/AIRQ				17.	N.C.
5.	/TIRQ				16.	N.C.
6.	CE				15.	N.C.
7.	CLK				14.	N.C.
8.	DI				13.	GND
9.	DO	#10		#11	12.	GND
10.	V_{DD}				11.	FOUT

VSOJ - 20 pin

3.2.Pin functions

Pin name	Pin number	I / O *1	Functions
V_{DD2} *2	1	–	RTC power (backup power). This pin is connected to the plus side of the power. (Always supply the power irrespective of action situation to this terminal.)
VEX *2	2	AIN	External voltage detection input pin. If external voltage decreases blow VEX,EXF bit became “1” . Note: This function acts only when V_{DD2} is supplied the power.
FOE	3	I	This is an input pin to control FOUT output. When the FOE pin is at the “H” level, the FOUT pin goes into the output state; when it is at the “L” level, the FOUT pin becomes Low.
/AIRQ	4	O.D.	This is the open drain output pin for alarm and time update interrupts.
/TIRQ	5	O.D.	This is the open drain output pin for timer interrupt.
C E	6	I	This is a chip enabled input pin with the built-in pull-down resistor. When the CE pin is at the “H” level, access to this RTC becomes possible. When the CE pin is at the “L” level, the DO pin is at the high impedance level, and the CLK and DI pins would not accept input.
CLK	7	I	This is the shift clock input pin for serial data transfer. In the write mode, it takes in data from the DI pin using the CLK signal rise edge. In the read mode, it outputs data from the DO pin using the fall edge.
DI	8	I	Serial data input pin
DO	9	O	Serial data output pin
V_{DD} *2	10	–	Main power. This pin is connected to the plus side of the power.
FOUT	11	O	This pin outputs the reference clock signal at 32.768 kHz (CMOS output). Depending on the level of the FOE input pin, output from the FOUT pin can be prohibited.
GND	12-13	–	This pin is connected to the minus side (ground) of the power.
N.C.	14 – 20	–	This pin is not connected to the IC chip. All the N.C. pins are connected collectively with the inside frame. Connect this pin to OPEN, GND, or V_{DD}.

*1) I: CMOS INPUT, O: CMOS OUTPUT, AIN: Analog INPUT, O.D.: Open Drain Output

*2) Be sure to connect a filter capacitor of at least 0.1 µF near V_{DD}–GND, V_{DD2}–GND and VEX–GND.

4. Absolute maximum ratings

GND=0 V

Item	Symbol	Condition	Rating	Unit
Power voltage	V_{DD}, V_{DD2}	V_{DD}–GND, V_{DD2}–GND	–0.3 to +6.0	V
Input voltage	V_{IN}	Input pin	GND–0.3 to V_{DD}+0.3	V
	V_{AIN}	VEX pin	GND–0.3 to +6.0	
Output voltage	V_{OUT}	/AIRQ, /TIRQ, FOUT, DO pins	GND–0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	Stored bare product after unpacking	–55 to +125	°C

5. Recommended operating conditions

GND=0 V

Item	Symbol	Condition	Rating	Unit
Operating power voltage	V_{DD}	V_{DD} pin	2.7 to 3.6	V
RTC power voltage	V_{DD2}	V_{DD2} pin	1.8 to 5.5	V
Analog power voltage	V_{EX}	VEX pin	1.4 to 5.5	V
Operating temperature	T_{OPR}	No condensation	-40 to +85	°C

6. Frequency characteristics

GND=0 V

Item	Symbol	Condition	Rating	Unit
Frequency accuracy / Clock accuracy	$\Delta f / fo$	Ta= +25 °C V_{DD2}=3.0 V	5 ± 23 (*1)	$\times 10^{-6}$
Frequency voltage characteristics	f / V	Ta= +25 °C V_{DD}=1.8 V to 5.5 V	± 2 Max.	$\times 10^{-6}$ / V
Frequency temperature characteristics	Top	Ta= –20 °C to +70 °C V_{DD}= 3.0 V ; reference at +25 °C	+10 / –120	$\times 10^{-6}$
Oscillation start up time	t_{STA}	Ta= +25 °C V_{DD}=3.0 V	3 Max.	s
Aging	fa	Ta= +25 °C V_{DD}=3.0 V ; first year	± 5 Max.	$\times 10^{-6}$ / year

*1) Equivalent to 1 minute of monthly deviation (excluding offset).

7. DC Electrical characteristics

*If not specifically indicated, V_{DD}=2.7 V to 3.6 V, V_{DD2}=1.8 V to 5.5 V, GND=0 V, Ta= –40 °C to +85 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
V_{DD} current consumption	I_{DD1}	V_{DD}=3.0 V, FOUT; output OFF			0.2	3.0	µA
	I_{DD2}	V_{DD}=3.0 V, CL=0 pF, FOUT; 32.768 kHz output ON			1.0	3.5	
V_{DD2} current consumption	I_{BK1}	V_{DD2}=3.0 V, FOUT; output OFF			0.8	1.0	µA
	I_{BK2}	V_{DD2}=3.0 V, CL=0 pF, FOUT; 32.768 kHz output ON			0.8	1.0	
"H" input voltage	V_{IH}	CE, CLK, DI, FOE pin		0.8V_{DD}		V_{DD}	V
"L" input voltage	V_{IL}	CE, CLK, DI, FOE pin		0		0.2V_{DD}	V
"H" Output voltage	V_{OH1}	FOUT pin	I_{OH} = –1 mA	V_{DD}–0.4		V_{DD}	V
	V_{OH2}	DO pin	I_{OH} = –1 mA	V_{DD}–0.4		V_{DD}	
"L" Output voltage	V_{OL1}	FOUT pin	I_{OL} = 1 mA	GND		GND+0.4	V
	V_{OL2}	DO pin	I_{OL} = 1 mA	GND		GND+0.4	
	V_{OL3}	/AIRQ, /TIRQ pin	I_{OL} = 2 mA	GND		GND+0.4	
Input resistor	R_{DWN}	CE, FOE pin	V_{IN} = V_{DD} or GND	75		600	kΩ
Input leakage current	I_{LK}	CE, CLK, DI, FOE pin	V_{OUT} = V_{DD} or GND	–0.5		0.5	µA
Output leakage current	I_{OZ}	DO, /AIRQ, /TIRQ, FOUT pin	V_{IN} = V_{DD} or GND	–0.5		0.5	µA

8. AC Electrical characteristics

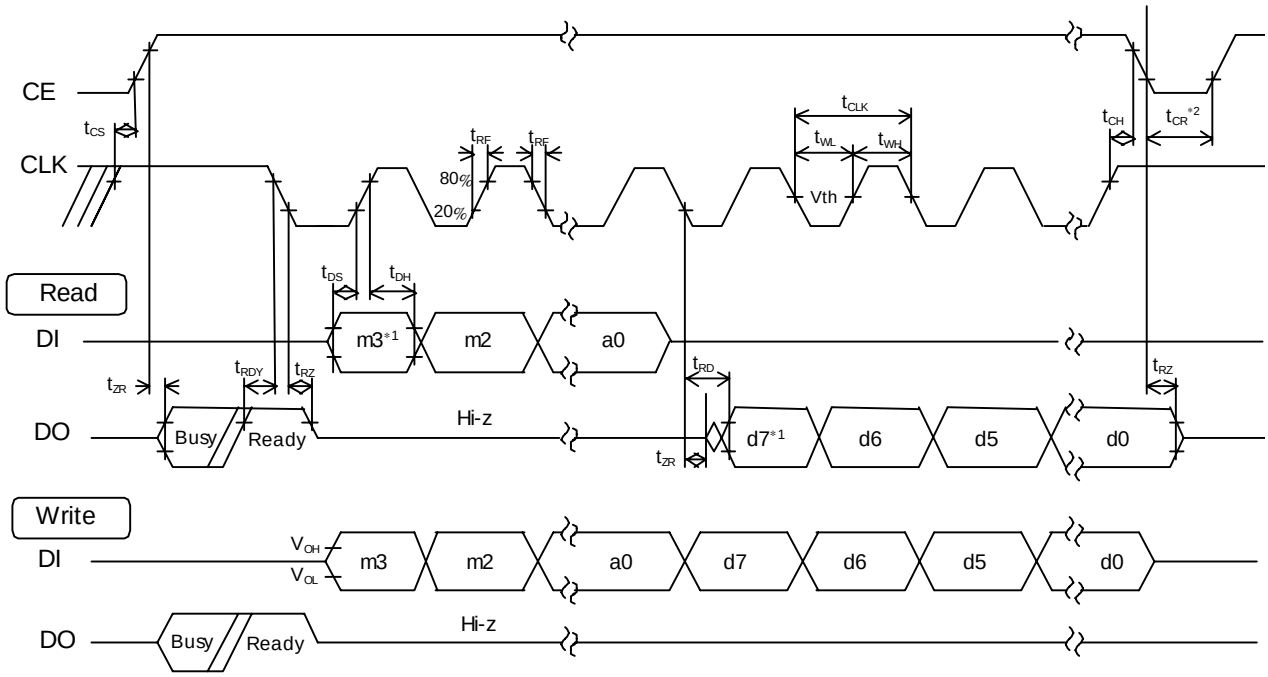
*If not specifically indicated, V_{DD}=2.7 V to 3.6 V, V_{DD2}=1.8 V to 5.5 V, GND=0 V, Ta= –40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK clock cycle	t_{CLK}	Vth = 50% V_{DD}	500			ns
CLK H pulse width	t_{WH}	Vth = 50% V_{DD}	230			ns
CLK L pulse width	t_{WL}	Vth = 50% V_{DD}	230			ns
CE setup time	t_{CS}		110			ns
CE hold time	t_{CH}		170			ns
CE recovery time	t_{CR}		350			ns
Write data setup time	t_{DS}		150			ns
Write data hold time	t_{DH}		150			ns
Read data delay time	t_{RD}	C_L = 65 pF ± 10 pF			240	ns
DO output switching time	t_{ZR}	C_L = 65 pF ± 10 pF	170			ns
DO output disable time	t_{RZ}	C_L = 65 pF ± 10 pF R_L = 10 kΩ			240	ns
Ready setup time	t_{RDY}		65			ns
CLK rise and fall time	t_{RF}	20 % ~ 80 % of V_{DD}			30	ns
Carry Busy *1	t_{carry}	X'tal = 32.768 kHz			7.8125	ms
FOUT Duty	tw / t	Vth = 50% V_{DD} V_{DD} = 3.0V	40	50	60	%

*1) Since "writing to EEPROM: twnv" and "performing carry action: tcarry" are OR output, maximum of 17.8125ms Busy signal output.

Read & Write Timing

With exception of data transfer at initial power supply and at voltage decrease of V_{DD2}, hold the carry operation when transfering data, so that the DO pin will output the Busy signal (0:Busy / 1:Ready) right after communication starts (CE=HIGH). If it's at the Ready state, communication is permitted. If it's at the Busy state, either the clock is being updated or the EEPROM Memory is being written. In this case, wait until it becomes Ready, or stop communication (CE=LOW) once to restart some time after. By any chance a data is transferred when it is at the Busy state, that data is not guranteed to be safe. The Busy signal becomes Hi-z at the timing when the initial rise edge of the clock occurs.



*1) The address width and the data width in the RTC mode differs for those in the EEPROM Memory mode.
*2) If the Busy/Ready signal is ignored, make sure to reserve 16 ms at least once every second.
*3) Latch data at the positive edge. (Data is output at the Negative Edge of clock signal.)
*4) Since the registers are undefined at initial power supply as well as after voltage decrease of V_{DD2}, the Ready signal may not output. After power supply, reserve more than 20ms, and then check the Busy / Ready signal. If the Ready signal is not output in more than 17.8125 ms, access by ignoring the Busy signal and initialize all the registers.

9. Voltage detection characteristics

9.1. VEX voltage detection characteristics

*If not specifically indicated, V_{DD}=2.7 V to 3.6 V, V_{DD2}=1.8 V to 5.5 V,GND=0 V, Ta= –40 °C to +85 °C

Item	Signal	Condition	Min.	Typ.	Max.	Unit
Current consumption	I_{DDVEX}	V_{EX} = 3.0 V	10	20	40	µA
Operation voltage for detection circuitry	V_{EX}	VEX pin	2.3	2.5	2.7	V
Hysteresis voltage	V_{HYS}		70	120	170	mV
Low active voltage	V_{ACT}	I_{OL} = 1 mA , V_{OL} = 0.4 V	1.4			V

* Be sure to connect a filter capacitor of at least 0.1 µF near VEX–GND.

9.2. VLF voltage detection characteristics

*If not specifically indicated, V_{DD}=2.7 V to 3.6 V, V_{DD2}=1.8 V to 5.5 V,GND=0 V, Ta= –40 °C to +85 °C

Item	Signal	Condition	Min.	Typ.	Max.	Unit
Current consumption	I_{DDVLF}	VLF constant enable	3	10	30	µA
Operation voltage for detection circuitry	V_{LF}	V_{DD2} pin	1.4	1.8	2.2	V

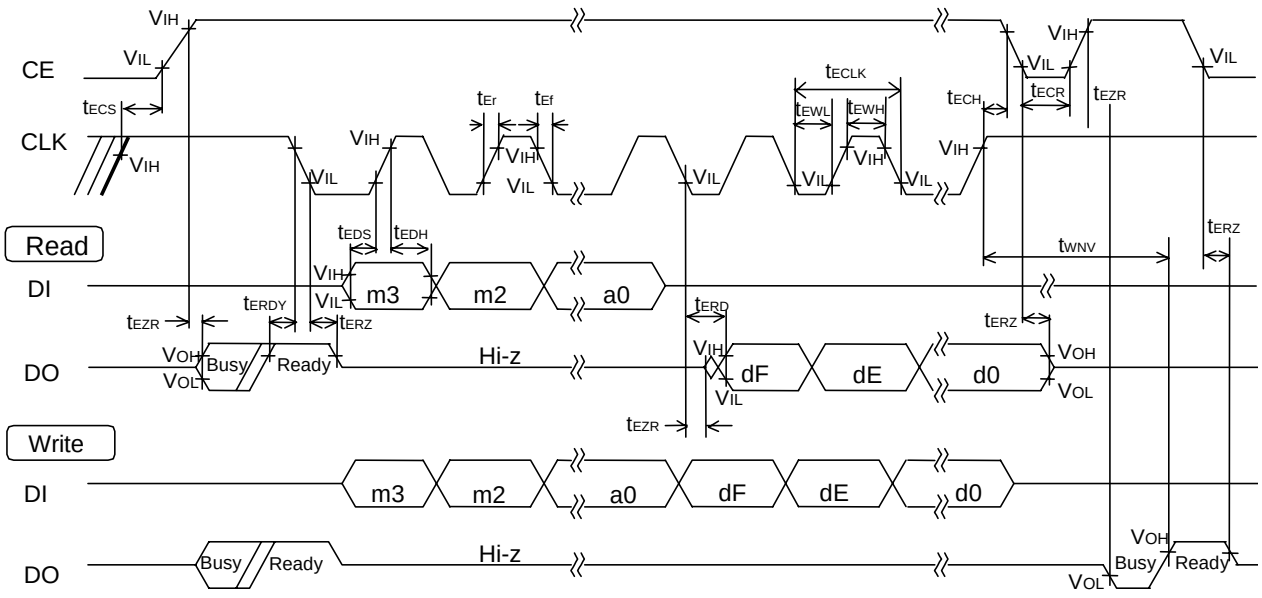
10. EEPROM Memory characteristics

* If not specifically indicated,GND=0 V, V_{DD}=2.7 V to 3.6 V, V_{DD2}=1.8 V to 5.5 V, Ta=-40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Memory configuration			4 kbit (256 × 16 bit)			–
Program/Erase cycle			10^5			times
Current consumption	I_{DD3}	Write to EEPROM		1	3	mA
Access time	t_{WNV}			5	10	ms
CLK clock cycle	t_{ECLK}	V_{DD} = 3.0 V ± 0.3 V	1000			ns
		V_{DD} = 3.3 V ± 0.3 V	900			ns
CLK H pulse width	t_{EWH}		430			ns
CLK L pulse width	t_{EWL}		430			ns
CE setup time	t_{ECS}		110			ns
CE hold time	t_{ECH}		150			ns
CE recovery time	t_{ECR}		350			ns
Write data setup time	t_{EDS}		150			ns
Write data hold time	t_{EDH}		160			ns
Read data delay time	t_{ERD}	C_L = 65 pF ± 10 pF			240	ns
DO output switching time	t_{EZR}	C_L = 65 pF ± 10 pF	170			ns
DO output disable time	t_{ERZ}	C_L = 65 pF ± 10 pF R_L = 10 k			240	ns
Ready setup time	t_{ERDY}		65			ns
Input rise and fall time	t_{Er},t_{Ef}	20 % to 80 % of V_{DD}			30	ns

* Power for the EEPROM Memory is supplied from V_{DD}. In order to turn the power OFF after writing, make sure to save t_{WNV} before turning the power OFF.

EEPROM Memory Timing (Post Write Check)



11. Register table

11.1. Register table

11.1.1. RTC register table (when the RTC mode is set)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	Comments
0	SEC	○ *1	S40	S20	S10	S8	S4	S2	S1	R/W	BCD notation
1	MIN	○	M40	M20	M10	M8	M4	M2	M1	R/W	BCD notation
2	HOUR	○	○	H20	H10	H8	H4	H2	H1	R/W	BCD notation
3	WEEK	○	W6	W5	W4	W3	W2	W1	W0	R/W	2^n notation
4	DAY	○	○	D20	D10	D8	D4	D2	D1	R/W	BCD notation
5	MONTH	○	○	○	C10	C8	C4	C2	C1	R/W	BCD notation
6	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	R/W	BCD notation
7	Y100 *2	0	0	1	0	0	0	0	0	R	20 is fixed (BCD)
8	MIN Alarm	AE	MA40	MA20	MA10	MA8	MA4	MA2	MA1	R/W	BCD notation
9	HOUR Alarm	AE	○	HA20	HA10	HA8	HA4	HA2	HA1	R/W	BCD notation
A	WEEK Alarm	AE	WA6	WA5	WA4	WA3	WA2	WA1	WA0	R/W	WADA=0
	DAY Alarm		○	DA20	DA10	DA8	DA4	DA2	DA1		WADA=1
B	Reserved *3	Reserved								R/W Prohibition	R/W Prohibition
C	Interval Timer	TDUTY	CT6	CT5	CT4	CT3	CT2	CT1	CT0	R/W	–
D	Extension Reg.	TEST *4	WADA	UDUTY	USEL	○	○	TSEL1	TSEL0	R/W	–
E	Flag Reg. *5	VLF2	○	UF	TF	AF	EXF	VLF	○	R/W	–
F	Control Reg.	○	○	UIE	TIE	AIE	EXIE	VLIE	○	R/W	–

Note1. 1. At the initial power supply, the values of the registers are not fixed, so please initialize them before use. While initializing, do not set impossible data for date and time; otherwise there is no guarantee that the clock will operate properly.

Note2. ∗1.“0” is read where “○” is marked. When writing data, use “0”.
∗2. Since these are read-only bits, write is not permitted.
∗3. The Resreved register used by EPSON for testing. Setting does not do.
∗4. The TEST bit is used by EPSON for testing. Be sure to set it to "0" before use.
∗5. The flag bit will cleared with “0”. (“0” can not be replace to “1”.)

11.1.2. EEPROM Memory table (When EEPROM Memory mode is set.)

Segment	Address	Data																Comments
		dF	dE	dD	dC	dB	dA	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	
0	00 ⋮ FF	User Memory																4 kbit (256 × 16 bit)

11.2. Description of RTC functions (addresses between 0 and 7)

The clock and the caledar consists of seconds, minutes, hours, day of the week, day, month, year and every 100 year (SEC, MIN, HOUR, WEEK, DAY, MONTH, YEAR and Y100 registers).

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	Comments
0	SEC	○	S40	S20	S10	S8	S4	S2	S1	R/W	BCD notation
1	MIN	○	M40	M20	M10	M8	M4	M2	M1	R/W	BCD notation
2	HOUR	○	○	H20	H10	H8	H4	H2	H1	R/W	BCD notation
3	WEEK	○	W6	W5	W4	W3	W2	W1	W0	R/W	
4	DAY	○	○	D20	D10	D8	D4	D2	D1	R/W	BCD notation
5	MONTH	○	○	○	C10	C8	C4	C2	C1	R/W	BCD notation
6	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	R/W	BCD notation
7	Y100	0	0	1	0	0	0	0	0	R	20 is fixed (BCD)

11.2.1. SEC register and MIN register (addresses 0 and 1)

These registers are 60-base BCD counters.

These registers are incremented at the timing when carry is generated from a lower register. At the timing when the lower register changes from 59 to 00, carry is generated to the higher register and thus incremented. (If inappropriate value (like 65) is set, the SEC/MIN register is cleared to “00” (at the increment) and carry may be generated to the higher register.)

When data is written to the MIN register, all the counters lower than it are cleared. Clearing occurs right after CLK data latch of D0 data.

11.2.2. HOUR register (address 2)

This register is a 24-base BCD counter (24 hour format).

This register is incremented at the timing when carry is generated from the MIN register. At the timing when this register changes from 23 to 00, carry is generated to the WEEK register and the DAY register.

	24h format											
a.m.	00	01	02	03	04	05	06	07	08	09	10	11
p.m.	12	13	14	15	16	17	18	19	20	21	22	23

11.2.3. WEEK register (address 3)

This register is a septenary BCD counter (counts from 0 to 6). It is incremented when carry is generated from the HOUR register. This register does not generate carry to a higher register. Since this register is not connected with the YEAR, MONTH and DAY registers, it needs to be set again with the matching day of the week if any of the YEAR, MONTH or DAY registers have been changed. As in the WEEK alarm register, this register is in 2^n format.

Day of the week	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		W6	W5	W4	W3	W2	W1	W0
Sunday	○	0	0	0	0	0	0	1
Monday	○	0	0	0	0	0	1	0
Tuesday	○	0	0	0	0	1	0	0
Wednesday	○	0	0	0	1	0	0	0
Thursday	○	0	0	1	0	0	0	0
Friday	○	0	1	0	0	0	0	0
Saturday	○	1	0	0	0	0	0	0

* Be careful not to write “1” to multiple bits.

11.2.4. DAY register and MONTH register (addresses 4 and 5)

The DAY register is a variable (between 28-base and 31-base) BCD counter that is influenced by the month and the leap year. It is incremented when carry is generated from the lower register. (If inappropriate values are set for day and month, the DAY register is set to 01 (at increment) and carry may be generated to the higher register.)

DAY register: 01 to 28, 29, 30, or 31 (depending on the month and the leap year)
MONTH register: 01 to 12

		Jan.	Feb.	March	April	May	June	July	Aug.	Sep.	Oct.	Nov.	Dec.
Last day	Normal year	31	28	31	30	31	30	31	31	30	31	30	31
	Leap year		29										

11.2.5. YEAR register (address 6 and 7)

This register is a BCD counter for years 2000 to 2099. The YEAR register is extended to display the year directly. Also, the leap year is automatically determined, which reflects in the DAY register.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	Comments
6	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	R/W	BCD notation
7	Y100	0	0	1	0	0	0	0	0	R	20 is fixed (BCD)

* Leap year is a year that can be divided by four (multiples of 100 is excluded except multiples of 400).

11.3. Alarm functions (/AIRQ)

From the conditions of the event flags (AF, EXF, VLF and VLF2), you can know the conditions when the clock matches, when the voltage decreases and when the oscillation stops. The data of these bits are kept until cleared with “0”. Also, since output to /AIRQ is possible when each event (except VLF2) is generated, interrupt can be requested to the host.

Since the value of the register is initially indeterminate at the initial power supply, the /AIRQ pin may output "L"(Active Low). Always initialize before use.

11.3.1. Time alarm (addresses between 8 and A)

11.3.1.1. Explanation of Time alarm (1).

When the registers corresponding to the minute, the hour, and the day of the week matches with the clock (comparing it right after carry is generated 7.8125 ms later), the alarm matching flag (AF) becomes “1”. At this moment, if the AIE (Alarm Interrupt Enable) is enabled (“1”), the /AIRQ pin outputs Active Low.

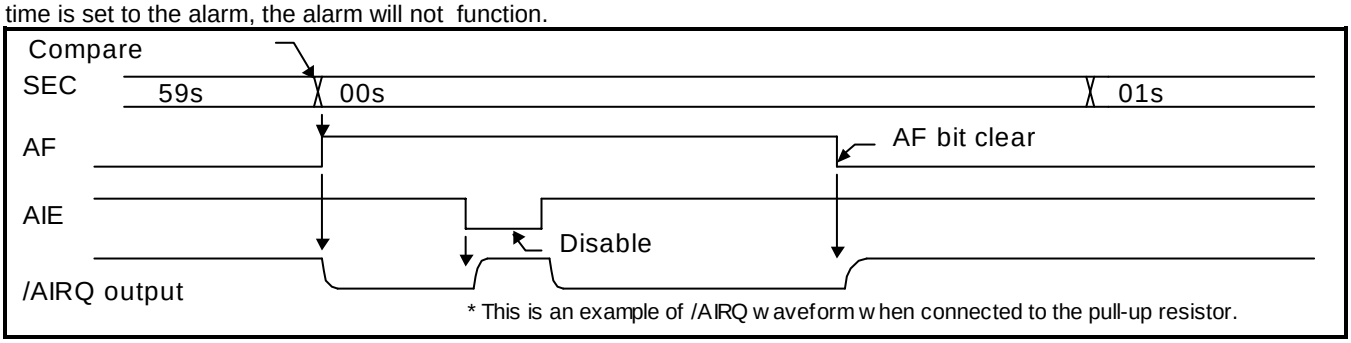
With the AE bit (bit 7: the Alarm Enable Don’t care bit) of each alarm registers, the HOUR alarm and the DAY alarm can be set. For the day of the WEEK alarm, multiple days can be set (i.e. Saturdays and Sundays). The WADA bit specifies the alarm to use between the WEEK alarm and the DAY alarm.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	Comments
8	MIN alarm	AE	MA40	MA20	MA10	MA8	MA4	MA2	MA1	R/W	BCD notation
9	HOUR alarm	AE	○	HA20	HA10	HA8	HA4	HA2	HA1	R/W	BCD notation
A	WEEK alarm	AE	WA6	WA5	WA4	WA3	WA2	WA1	WA0	R/W	WADA=0
	DAY alarm		○	DA20	DA10	DA8	DA4	DA2	DA1		WADA=1
D	Extension reg.		WADA							R/W	
E	Flag reg.					AF				R/W	
F	Control reg.					AIE				R/W	

Bit name	Bit data	Function	Comments
AE	0	Compares the corresponding register	This is in negative logic, so be careful.
	1	Does not compare the corresponding register (don't care)	
AIE	0	/AIRQ output is prohibited	
	1	/AIRQ output (alarm interrupt is valid)	
AF	0	Alarm unmatched	-
	1	Alarm matched	This bit is kept until overwriting with “0”.
WADA	0	WEEK alarm is set	
	1	DAY alarm is set	

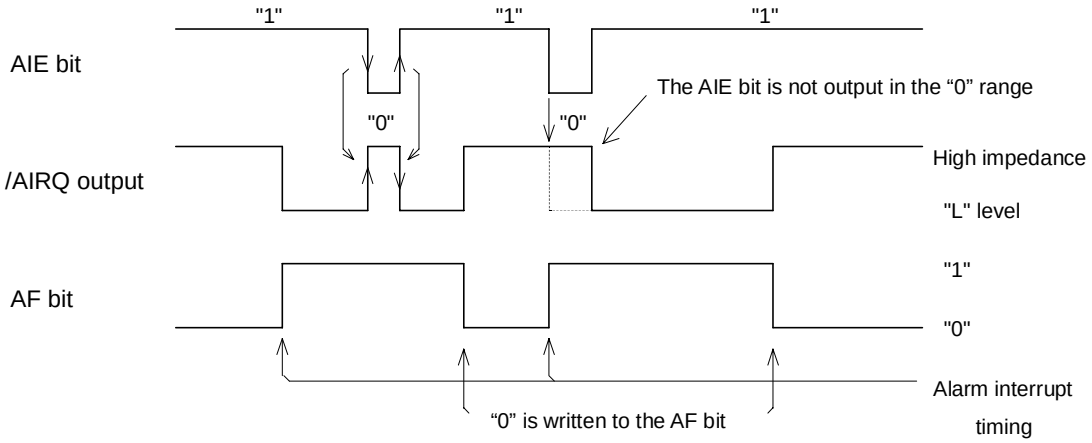
To avoid malfunction, the compare operation is halted while writing to the alarm registers. If write to the alarm register during this time (period of 7.8152 ms from carry occurrence), the alarm will not function.

The compare operation is performed during the carry operation (the interval of the lowest carry digit of the AE enabled register). If the AF bit is cleared exactly when the time matches the alarm data, the alarm will not function. Even if the current time is set to the alarm, the alarm will not function.



11.3.1.2. Explanation of Time alarm (2).

When the alarm matches and AIE=1, the /AIRQ pin outputs “L”; when AIE=0, the /AIRQ pin is at the high impedance level.



1) How to use

The day of the week, day, hours and minutes can be set. For the day of the week, multiple days can be set at one time. The WADA bit specifies which alarm is used between the WEEK alarm and the DAY alarm.

To avoid unintended hardware interrupt during the alarm setup, it is recommended that AIE bit be initially set to “0”. Then, set up the alarm data, and apply zero clear to the AF flag in order to initialize (with certainty) the alarm circuitry. Afterward, set the AIE bit to “1”. If you desire no hardware interrupt, set the AIE bit to “0”, and monitor the AF bit with software as required.

2) Usage example

a) Set the alarm to go off at 6 p.m. tomorrow (when the WADA bit specifies the WEEK alarm).

- Write “0” to the AIE bit and “0” to the AF bit.
- Write “0” to the WADA bit (selects the WEEK alarm).
- Write “1” to the AE bit of the WEEK/DAY alarm.
- Shift the current day of the week recorded in the WEEK alarm register 1 bit to the left, then write this data to the WEEK alarm register.
  (If bit 6 is set to “1” (Saturday), then write “01h” (Sunday).)
- Write “18h” to the HOUR alarm register.
- Write “00h” to the MIN alarm register.
- Clear the AF bit to zero.
- Write “1” to the AIE bit.

b) Set the alarm to go off at 6 a.m. every morning except Saturdays and Sundays.

- Write “0” to the AIE bit and “0” to the AF bit.
- Write “0” to the WADA bit (selects the WEEK alarm).
- Write “3Eh” to the WEEK alarm register.
- Write “06h” to the HOUR alarm register.
- Write “00h” to the MIN alarm register.
- Clear the AF bit to zero.
- Write “1” to the AIE bit.

11.3.2. Voltage detection function

11.3.2.1. VEX voltage decrease alarm (EXF)

With the voltage detection circuitry that is independent from the other power supplies, the VEX voltage can be monitored constantly. If the voltage decreases below VEX, EXF (V_{DD} Low alarm Flag) becomes "1" and /AIRQ (Interrupt Request) becomes Active Low. Even if the voltage recovers, this state is kept until EXF is cleared. Although this circuitry can constantly monitor the voltage in high precision, current is consumed, so be careful.

As chief usage, use it to monitor the voltage of the main battery (for the main power source).

Bit name	Bit data	Function	Comments
EXIE	0	VEX voltage monitor circuitry OFF	
	1	VEX voltage monitor circuitry ON (constantly)	
EXF		Read "1" : voltage is below VEX voltage	Kept until overwriting with "0"

11.3.2.2. V_{DD2} voltage decrease alarm (VLF)

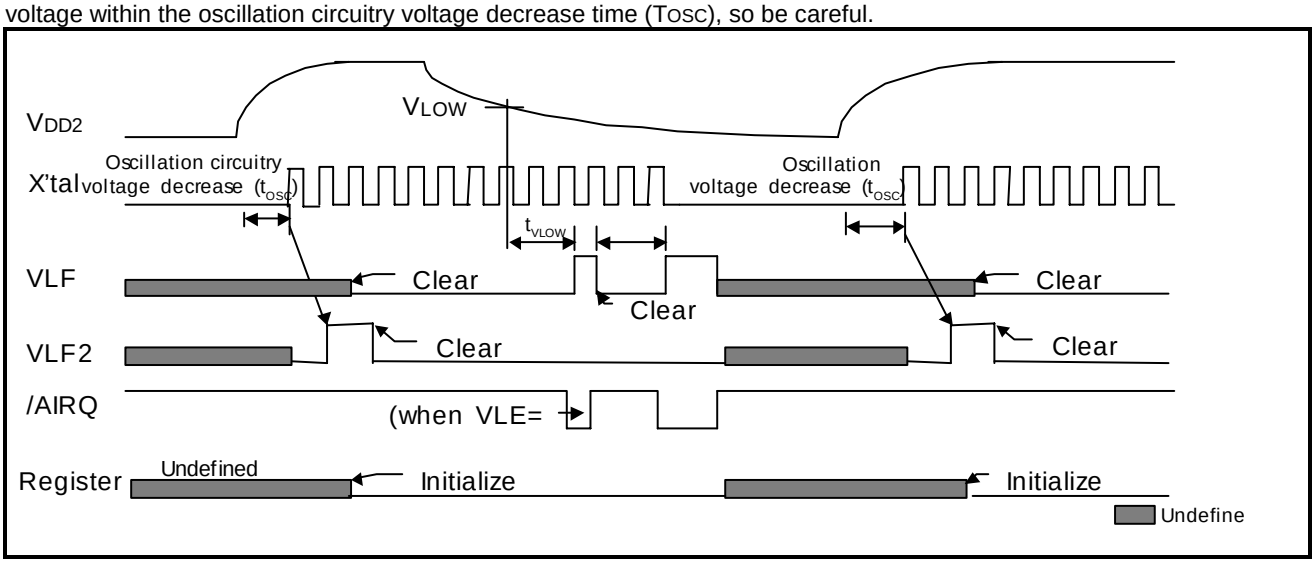
When the VLIE bit is enabled, the V_{DD2} voltage is monitored once every 10 seconds. During this time, if the voltage decreases below V_{LOW}, VLF (V_{DD2} Low alarm Flag) becomes "1" and /AIRQ (Interrupt Request) becomes Active Low. This state is kept until VLF is cleared. In this circuitry, if the VLIE bit is disabled, the current consumption may be suppressed to minimum, but the voltage monitor circuitry will not operate.

If the voltage decreases momenteraly for less than 10 seconds, VLF may not be detected, so be careful.

Bit name	Bit data	Function	Comments
VLIE	0	/AIRQ output is prohibited	V_{DD2} voltage monitor circuitry OFF
	1	/AIRQ output	V_{DD2} voltage monitor circuitry ON (once every 10 seconds)
VLF		Read "1" : V_{DD2} voltage is below V_{LOW} voltage	Kept until overwriting with "0"

11.3.2.3. Oscillation circuitry voltage decrease flag (VLF2)

This is a function to detect decrease in oscillation circuitry voltage. If there had been a previous decrease in oscillation circuitry, VLF2 becomes "1". (**/AIRQ will not operate with VLF2 function.**) When VLF2 is "1", all the registers except the EEPROM Memory are undefined, so please perform the initial setup. Also, VLF may not detect instantaneous decrease in voltage within the oscillation circuitry voltage decrease time (T_{OSC}), so be careful.



11.4. Timer function (/TIRQ)

Since the value of the register is initially indeterminate at the initial power supply, the /TIRQ pin may output "L"(Active Low). Always initialize before use.

11.4.1. 1.Variable interval timer

The interval period and Duty can be set for this interval timer. /TIRQ becomes “0” when TF is released or when the Duty period is expired. The data in TF is kept until it is cleared.

By setting Duty to ON, the current consumption of the pull-up resistor is minimized and intermittent operations on standby are trigger locked; such multipurpose usages become possible. Be careful with the cycle error at the initial cycle of the source clock, which occurs due to the asynchronous operation of the source clock with count start timing. The next cycle will be fixed. See 11.4.1.2. for the cycle error at the initial cycle.

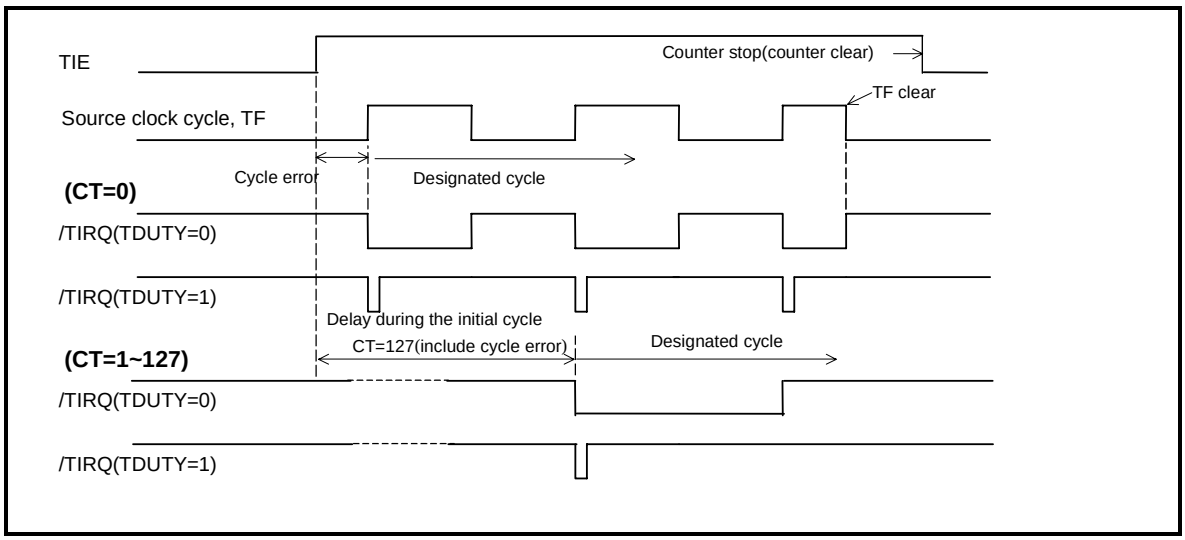
Addr	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	Comments
C	Interval timer	TDUTY	CT6	CT5	CT4	CT3	CT2	CT1	CT0	R/W	
D	Extension reg.							TSEL1	TSEL0	R/W	
E	Flag reg.				TF					R/W	
F	Control reg.				TIE					R/W	

Bit name			Function				Comments
TIE			0:/TIRQ output prohibited 1: /TIRQ out (interval timer interrupt is valid)				
TF			0:/TIRQ=Hi-Z 1: /TIRQ=Active Low				Opposite logic of /TIRQ
Source clock settings	TSEL1	TSEL0	Clock	Min.(CT=00 hex)	Max.(CT=7F hex)	Unit	
	0	0	1024 Hz	1/1024	128/1024	ms	Do not set Duty
	0	1	64 Hz	1/64	2	ms	
	1	0	1 Hz	1	128	s	TDUTY=0 (Duty =50 %)
	1	1	1 min	1	128	min	
	1	0	2 Hz	1/2	64	s	TDUTY=1 (Low width: 7.8125 ms)
	1	1	1 min	1	128	min	TDUTY=1 (Low width: 3.90625 ms)

11.4.1.2. How to use variable interval timer

If TIE has been set from “0” to “1” after the source clock and interval timer have been set, the initial cycle will not operate with the designated cycle.

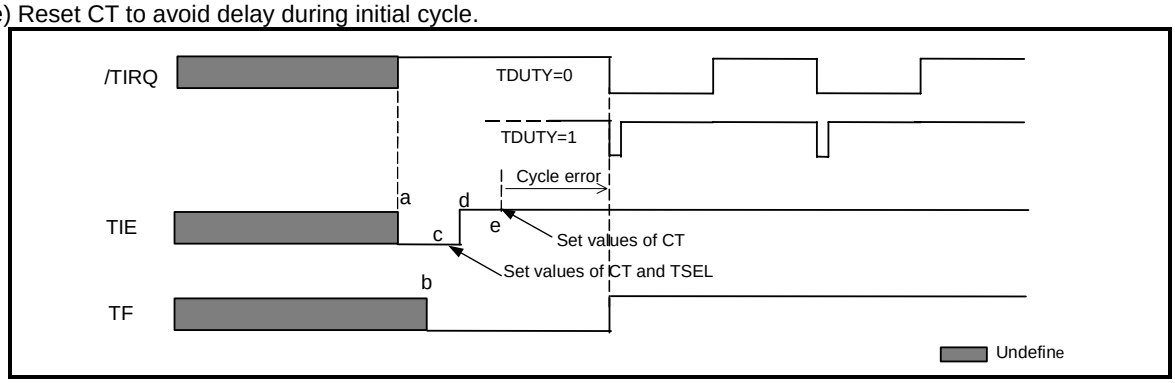
- If CT is set to 0, the cycle will be fixed after the cycle error in the initial cycle of the source clock.
- If CT is set to between 1 to 127, the interval timer will complete one cycle of length CT = 127, and then the cycle will be fixed. * See 11.4.1.3. for ways to avoid delay during the initial cycle.



11.4.1.3. Procedure for avoiding delay during initial cycle (if you set CT = 1 – 128)

By resetting CT after TIE is set to 1, the cycle will be fixed after CT reset.

(a) Set TIE to 0 to cancel output from /TIRQ.
(b) Set TF to 0 to clear flags.
(c) Set values of CT and TSEL (if CT = 0 when power is turned on, TIRQ may be output immediately after TIE is set to 1 if CT is not reset to some non-zero value.)
(d) Set TIE to 1.
(e) Reset CT to avoid delay during initial cycle.



11.4.2. Time update interrupt

Generates timer interrupt (/TIRQ) after time update of seconds or minutes. /TIRQ is released when UF is released or when Duty period is expired. The data in UF is kept until it is cleared.

By setting UDUTY to ON, the current consumption of the pull-up resistor is minimized

Addr	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	Comments
D	Extension reg.			UDUTY	USEL					R/W	
E	Flag reg.			UF	TF					R/W	
F	Control reg.			UIE	TIE					R/W	

Bit name	Bit data	Function	Comments
UIE	0	/TIRQ output is prohibited	-
	1	/TIRQ output	Default value
UF	0	-	-
	1	Clock update occurred	-
USEL	0	1s interrupt (at 1s carry)	-
	1	1min interrupt (at 00s)	Default value
UDUTY	0	50 % DUTY	-
	1	7.8125 ms or 3.90625 ms (low width)	Default value

11.5. Control register / Flag register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	Comments
D	Extension reg.	TEST	WADA	UDUTY	USEL	○	○	TSEL1	TSEL0	R/W	
E	Flag reg.	VLF2	○	UF	TF	AF	EXF	VLF	○	R/W	
F	Control reg.	○	○	UIE	TIE	AIE	EXIE	VLIE	○	R/W	

11.5.1. Control register

- TEST
  This bit is used by EPSON for testing. Be sure to set it to "0".
- WADA
  This bit sets either the WEEK alarm or the DAY alarm. For details, see the **Time alarm** section [11.3.1.].
- UDUTY, USEL, UIE
  This is the time update interrupt bit. For details, see the **Time update interrupt** section [11.4.2.].
- TSEL
  This is the source clock setting bit for the timer. For details, see the **Variable interval timer** section [11.4.1.].
- EXIE
  This is the enable bit for the VEX voltage decrease detection circuitry. For details, see the **VEX voltage decrease alarm** section [11.3.2.1.].
- VLIE
  This is the enable bit for the V_{DD2} voltage decrease detection circuitry. For details, see the **V_{DD2} voltage decrease alarm** section [11.3.2.2.].
- TIE
  This is the enable bit for the timer. For details, see the **Variable interval timer** section [11.4.1.1.].
- AIE
  This is the enable bit for the time alarm. For details, see the **Time alarm** section [11.3.1.].

11.5.2. Flag register

This register is the flag register. For each event (alarm and interval timer) generated, "1" is set. Set it to "0" to clear. To keep the corresponding register state, set it to "1" (mask).

- VLF2
  This bit is the flag that records oscillation circuitry voltage decrease. For details, see the **Oscillation circuitry voltage decrease flag (VLF2)** section [11.3.2.3.].
- UF
  This bit becomes "1" when time update occurs. For details, see the **Time update interrupt** section [11.4.2.].
- TF
  During the interval timer, this bit is set to "1" at the Negative Edge of the /TIRQ. For details, see the **Variable interval timer** section [11.4.1.1.].
- EXF
  This bit becomes "1" when VEX voltage decrease occurs. For details, see the **VEX voltage decrease alarm** section [11.3.2.1.].
- VLF
  This bit becomes "1" when VDD2 voltage decrease occurs. For details, see the **V_{DD2} voltage decrease alarm** section [11.3.2.2.].
- AF
  This bit becomes "1" when time match alarm occurs. For details, see the **Time alarm** section [11.3.1.].

12. Read / Write data

12.1. Serial data transfer method

This is a serial data transfer method in 4 lines form (or 3 lines form). Mode, address and data are transferred in MSB-first in respective order.

The first 4 bits (called mode field) determines the mode and the data size of the other fields (address and data fields).

12.1.1. Mode field

- The first 4 bits determines the mode.

Mode field		m3	m2	m1	m0
		Read/Write	Reserved	BANK register	
Data bit	0	0 : write	0 *	00: RTC mode 01: Reserved 10: EEPROM Memory 11: Reserved	
	1	1 : read	0 *		

* Make sure m2 is set to “0”.

12.1.2. Address field and data field

- RTC mode (m1 bit =0)

Mode field	m3	m2	m1	m0				
Address field	a3	a2	a1	a0				
Data field	d7	d6	d5	d4	d3	d2	d1	d0

- EEPROM Memory mode (m1 bit =1)

Mode field	m3	m2	m1	m0				
Address field	seg3	seg2	seg1	a7				
	a6	a5	a4	a3	a2	a1	a0	0
Data field	dF	dE	dD	dC	dB	dA	d9	d8
	d7	d6	d5	d4	d3	d2	d1	d0

* Since segment bits (seg3 to seg1) are used for memory expansion, write “0” to them.

12.2. Reading/Writing in RTC mode.

For both reading and writing, after CE input rises, set the 4-bits mode, then specify the 4-bits address, and finally read or write in 8-bits units.

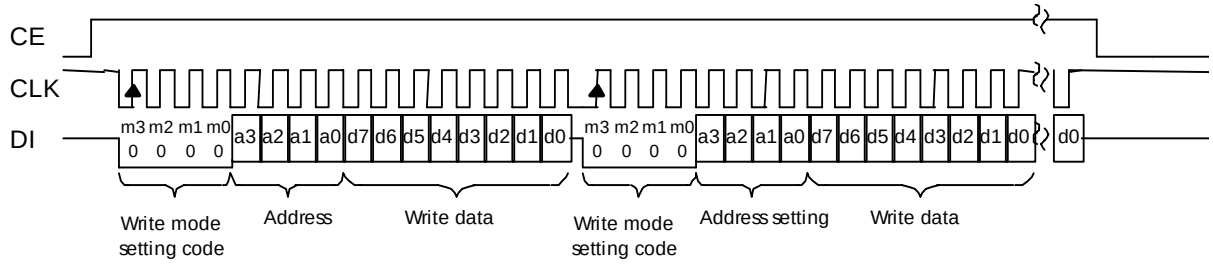
If the input of data in 8-bits unit is not completed before CE input falls, the 8-bits data will be ignored at the time CE input falls (the data before this is undefined).

Reading and writing both uses MSB-first.

12.2.1.Writing in RTC mode. (Cycle mode)

1) After CE input rises, set the first 4 bits (write mode setting code) to “1”, then write the address in the next 4 bits. Data is written in the following 8 bits.
2) The cycle mode can be used only when the RTC mode is set. Since read/write of data can be done continuously, this mode is useful to read the clock data and to overwrite (read/write) the flags (continuous access is limited to 1 second).

Example of writing.

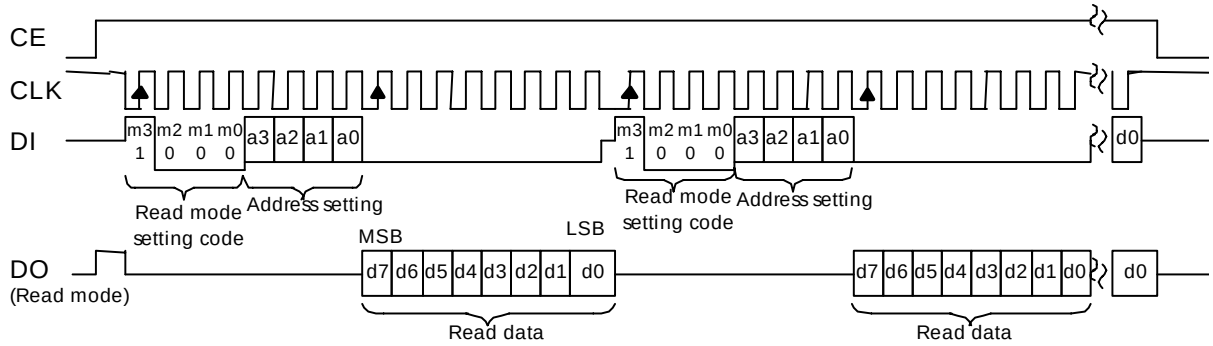


* While transferring data, switching to the EEPROM Memory mode is prohibited.

12.2.2. Reading in RTC mode.

1) After CE input rises, set the first 4 bits (read mode setting code) to “8”, then write the address data in the next 4 bits.
2) Read the address data, then read the following 8 bits.

Example of reading.



12.2.3. Write/Read setting code for each mode.

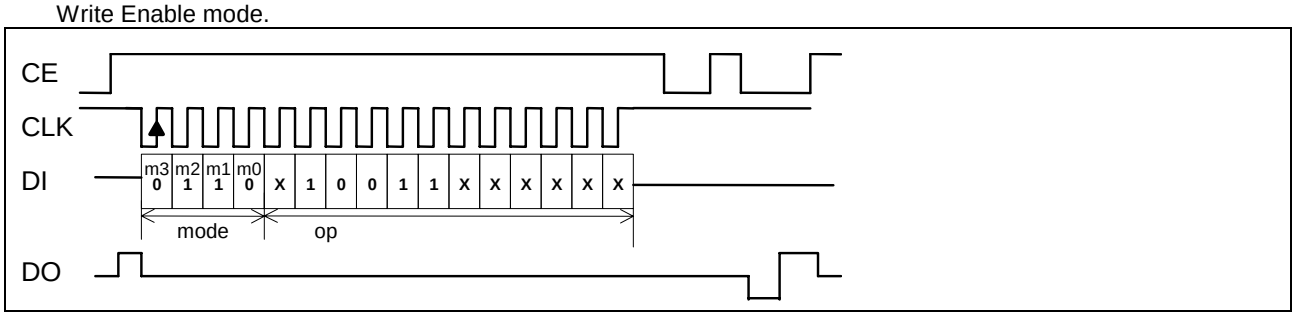
Mode	RTC
Write	0 h
Read	8 h

* Please do not set any mode setting code other than the ones in the table above.

12.3. Read / Write EEPROM Memory

12.3.1. Write Enable mode (EWEN)

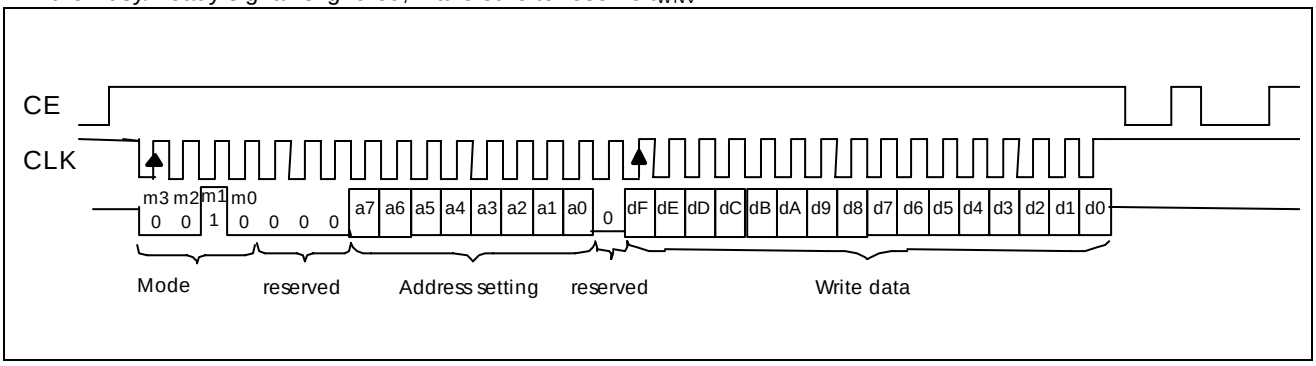
1) After power supply, please execute this once.
2) If data has been transferred while Busy, the Write Enable mode may be canceled. In this case, execute again the Write Enable mode.



12.3.2. Write EEPROM Memory

1) At power supply, set the Write Enable mode (Write Enable mode section [12.3.1.]).
2) After CE input rises, set the mode into the mode field (4 bits), and then make sure to set the segment bits (3 bits) of the address field to 0 because these are used for memory expansion. Set the address into the next 8 bits, and then set the following bit to "0". Finally, write the data in the data field.

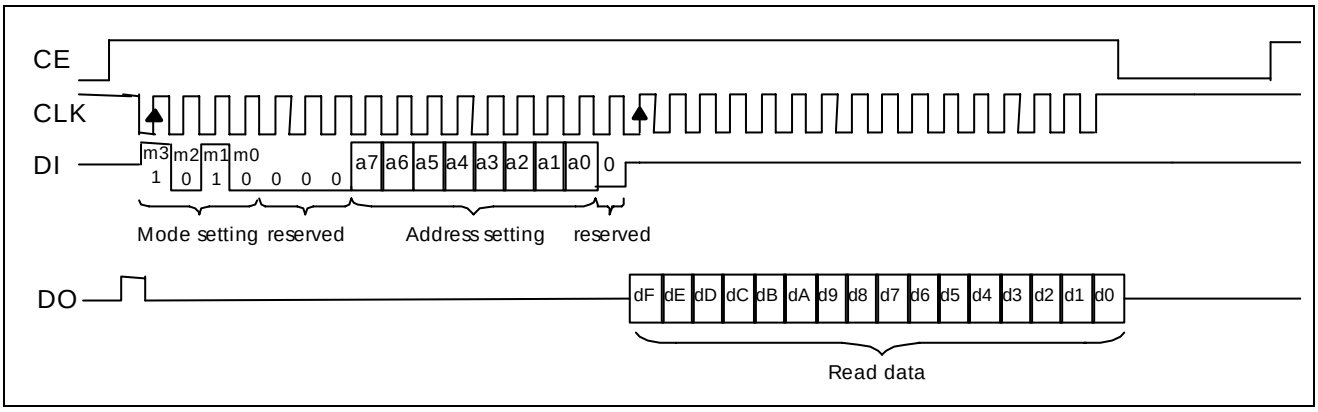
* If the Busy/Ready signal is ignored, make sure to reserve t_{WNV}.



12.3.3. Read EEPROM Memory

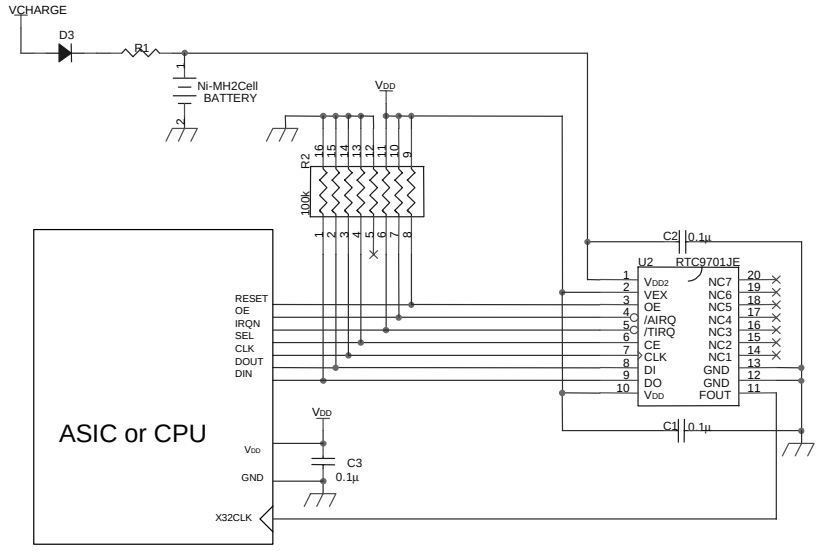
1) After setting the address, data can be transferred. This mode can be used only when the EEPROM Memory mode is set.
2) After CE input rises, set the mode into the mode field (4 bits), and then make sure to set the segment bits (3 bits) of the address field to 0 because these are used for memory expansion. Set the address into the next 8 bits, and then set the following bit to "0". The next 16 bits data is output from DO.

* If the Busy/Ready signal is ignored, make sure to reserve 16 ms once every second.



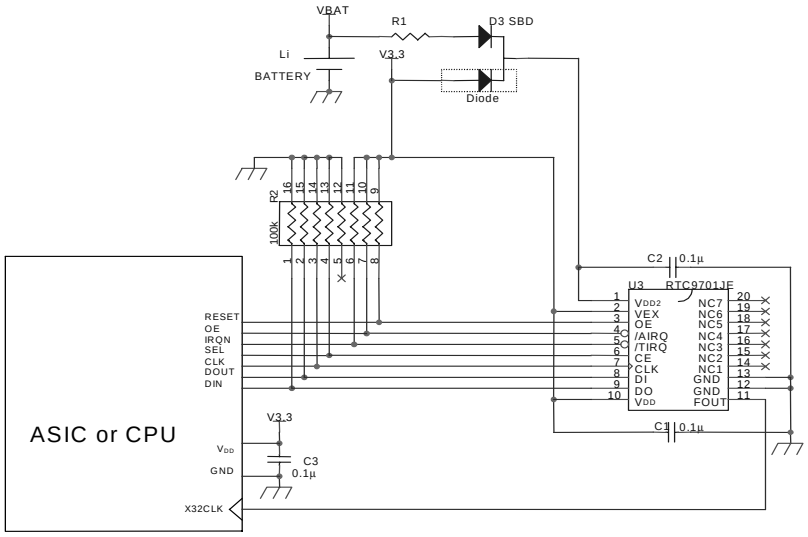
13. External connection examples

Example 1. Circuitry when using the secondary battery (trickle charge)



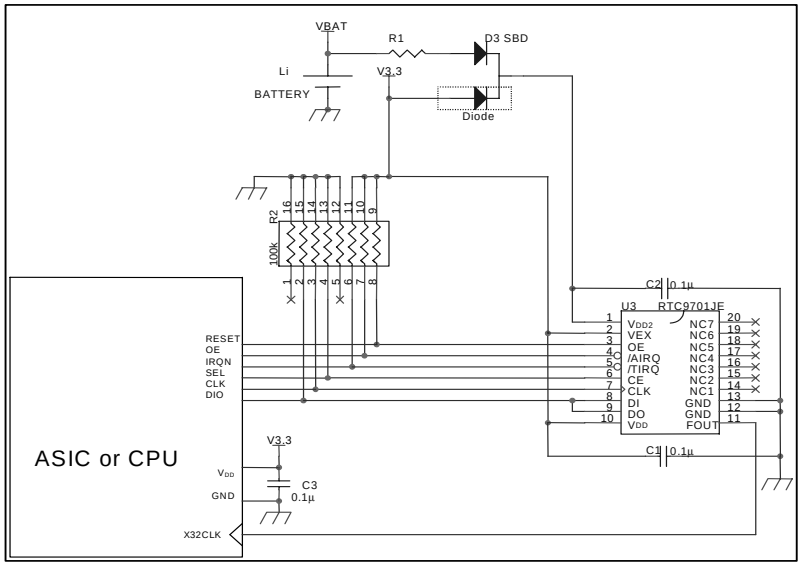
* If trickle charged, the R1 value will vary depending on the usage and the specification of the battery.

Example 2. Circuitry when using the primary battery



* For the safety purpose of the battery, mounting R1 and D3 is recommended.
* If the main power source and the diode is wired-OR, the consumption of the battery is reduced
(only when V_{BAT}<V3.3).

Example 3. Circuitry when DI pin and DO pin are wired-OR



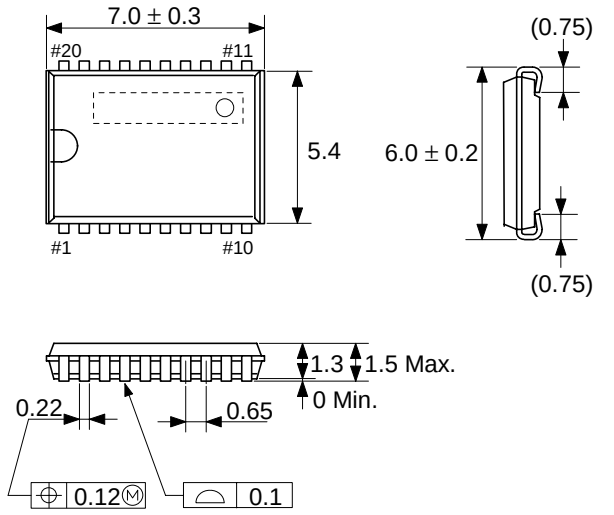
* For the safety purpose of the battery, mounting R1 and D3 is recommended.
* If the main power source and the diode is wired-OR, the consumption of the battery is reduced
(only when V_{BAT}<V3.3).

14. External diagram / Marking layout

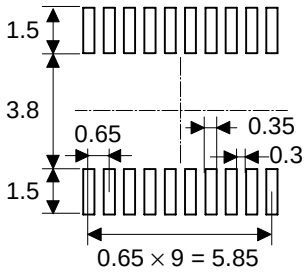
14.1. External diagram

RTC - 9701 JE (VSOJ-20pin)

• External dimensions



• Recommended soldering pattern

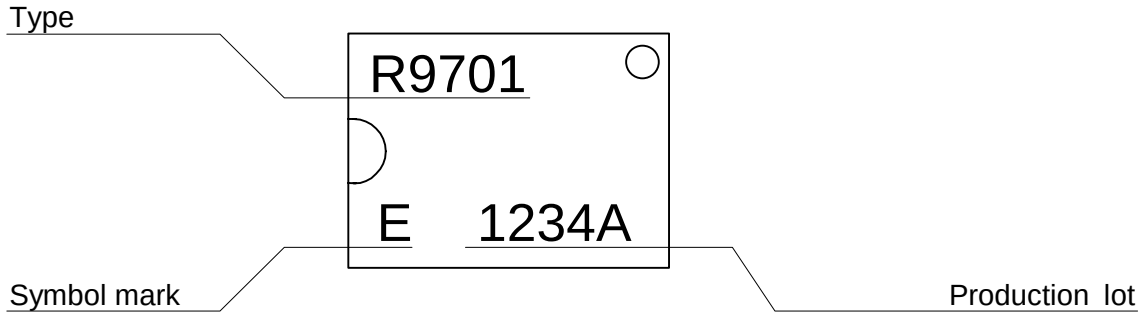


Unit : mm

* The cylinder of the crystal oscillator can be seen in this area (front and back), but it has no affect on the performance of the device.

14.2.Marking layout

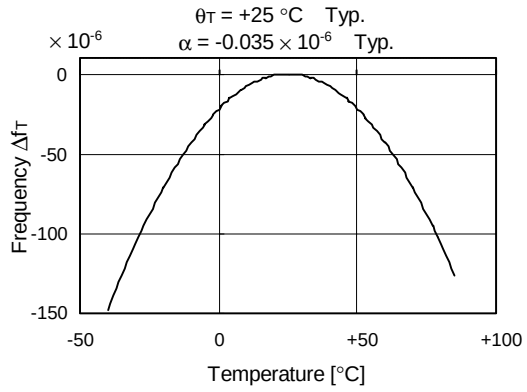
RTC - 9701 JE (VSOJ-20pin)



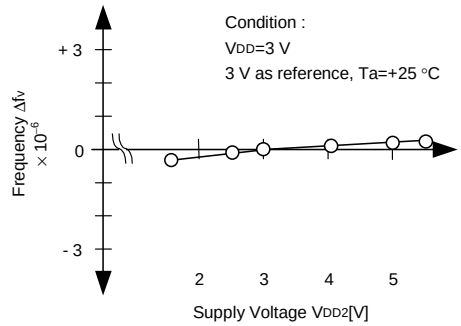
* The displayed content indicates the general markings and display, but are not the standards for the fonts, size and positioning.

15. Reference data

(1) Example of frequency and temperature characteristics



(2) Example of frequency and voltage characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta f_T = \alpha (\theta_T - \theta_X)^2$

Δf_T		: Frequency deviation in any temperature
α	($1 / °C^2$)	: Coefficient of secondary temperature ($-0.035 \pm 0.005) \times 10^{-6} / °C^2$
θ_T	(°C)	: Ultimate temperature (+25±5 °C)
θ_X	(°C)	: Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta f_T + \Delta fv$

$\Delta f/f$	: Clock accuracy (stable frequency) in any temperature and voltage
$\Delta f/fo$	: Frequency precision
Δf_T	: Frequency deviation in any temperature
Δfv	: Frequency deviation in any voltage

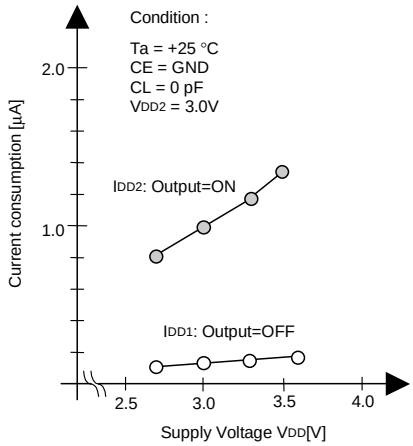
3. How to find the date difference

Date difference = $\Delta f/f \times 86400$ (seconds)

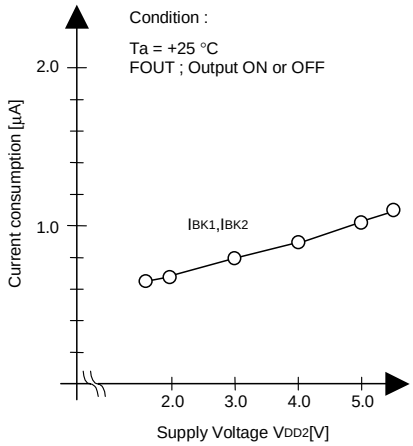
* For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

(3) Current and voltage consumption characteristics

(3-1) VDD Current consumption (IDD1, IDD2)



(3-2) VDD2 Current consumption (IBK1, IBK2)



16. Application notes

16.1. Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 µF as close as possible to the power supply pins (between V_{DD} and GND, between V_{DD2} and GND, and between VEX and GND). Also, avoid placing any device that generates high level of electronic noise near this module.

∗ Do not connect signal lines to the shaded area in the figure shown in Fig.1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to V_{DD} or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

16.2. Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1: Example of GND pattern

RTC - 9701 JE (VSOJ-20pin)

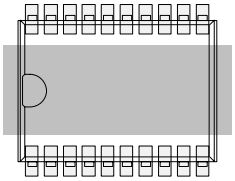
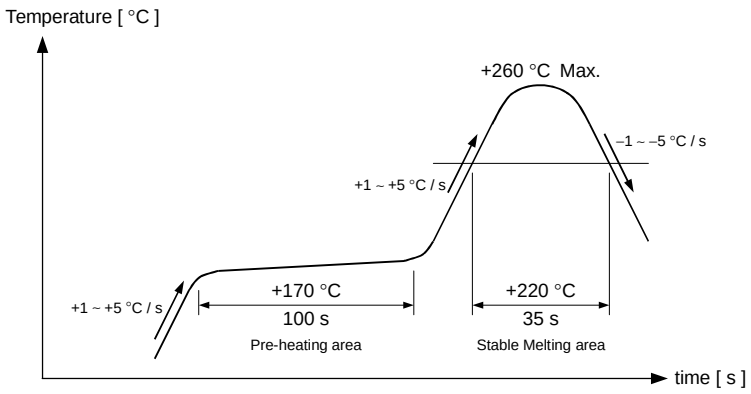


Fig. 2 : Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



EPSON TOYOCOM

Application Manual

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